Aswin Raj K

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WORK EXPERIENCE

Embedded Software Engineer II Jan 2025 – Present

Quasistatics Inc.

- **Led** firmware development across multiple Quasistatics chip portfolio - QS127, QS127S, QS221, QS222, and QS223 (newest variant) - spanning pre-silicon to post-silicon validation, including ARM Cortex bring-up, peripheral initialization, and feature development across all chips.
- **Developed** firmware on FreeRTOS and Zephyr RTOS across multiple platforms, leveraging Ambiq, Nordic NRF, and STM32 SDKs to implement peripheral drivers, interrupt handling, and hardware abstraction layers for each chip variant.
- **Owned** PTT (Push-To-Talk) firmware end-to-end for various WiR demo applications, successfully reducing sidetone latency to 20 ms. Resolved 10+ functional and timing bugs, incorporating customer feedback, and delivering improved firmware stability with a measurable reduction in recurring customer-reported regressions.
- **Designed** and implemented a Controlled Bit Error Testing framework for QS127S, increasing baseband validation coverage by ~40% and surfacing IC-level encoding/decoding and SPI bugs that significantly accelerated IC team root-cause resolution.
- **Established** pre- and post-silicon firmware environments for QS222 and executed a full knowledge transition to a new team member, cutting onboarding ramp-up time by an estimated 50%.
- **Collaborated** cross-functionally with hardware and IC teams across 4+ concurrent chip projects, translating debug findings into firmware fixes and improving first-pass validation rates.

Research Scholar Aug 2024 – Dec 2024

NYU NanoFab | New York, USA

- **Engineered** a centralized tool management system to monitor critical status signals for 4 pieces of NYU NanoFab equipment, improving system uptime reporting accuracy by 25%.
- **Implemented** a Python-based server to process telemetry from IoT modules, leveraging Modbus TCP/IP and CAN Bus protocols for robust machine-to-server communication with high data reliability.
- **Developed** custom C++ firmware for 4 types of embedded IoT devices to interface with laboratory hardware, ensuring high-fidelity data acquisition at a 10 Hz rate.
- **Designed** and deployed a remote monitoring GUI in Python, streamlining equipment accessibility and reducing the need for manual equipment checks.

ECE Graduate Assistant Sept 2023 – May 2024

NYU Nano Electronics Lab | New York, USA

- **Developed** an IoT device for real-time compressor status monitoring in dilution refrigerators, reducing unplanned downtime by enabling proactive fault detection.
- **Designed** and verified multi-layer PCBs for analog IC testing (256+ pins) with stringent low-noise tolerances, reducing signal interference by 18%.
- **Automated** data acquisition and analysis pipelines in Python using multithreading and multiprocessing, cutting manual data processing time and improving experimental throughput.
- **Implemented** systematic debugging workflows that reduced hardware/software downtime by 20% and recovered 10+ hours of system uptime per week.

Avionics and Software Testing Intern Jun 2021 – Sept 2021

Airbus Group India Pvt. Ltd. | Karnataka, India

- **Led** the migration of EZFAP from VBA to G Suite, optimizing tool performance and cutting daily processing time by 2 hours - a 25%+ productivity gain.
- **Executed** over 100 test cases for avionics software, ensuring compliance with industry standards and reducing software errors by 15%.
- **Collaborated** with cross-functional teams across avionics and software disciplines, contributing to on-time delivery of all assigned project milestones.

EDUCATION

New York University Sept 2022 – May 2024

MS in Electrical Engineering | GPA 3.9/4 | New York, USA

Indian Institute of Technology Palakkad May 2018 – May 2022

BTech in Electrical Engineering | GPA 8.98/10 | Kerala, India

SKILLS

Firmware & Embedded: C/C++, Assembly, ARM Cortex-M, Real-Time Debugging, FreeRTOS, Zephyr RTOS, Peripheral Drivers, NRF SDK, Ambiq SDK, STM32Cube
Digital & ASIC Design: RTL Design, Verilog, OpenLANE, ASIC Design Flow, GDS-II Tape-out, SDC Constraints, Cadence Virtuoso, Synopsys VCS, Cadence Genus
Hardware & PCB Design: Multi-layer PCB Design, Schematic Capture, Analog IC Testing, Low-Noise Tolerances, Allegro PCB Editor, Altium, IoT
Programming & Tools: Python (Async, Multithreading), C/C++, MATLAB, Simulink, Vivado, Git

PROJECTS

Smart Watch with Wi-R Bring-Up (Pebble OS) Jan 2025 – Present
Quasistatics Inc.

- **Led** firmware bring-up of the WiR chip on a smartwatch platform running Pebble OS, establishing chip communication, configuring peripheral interfaces, and achieving stable wireless functionality across all core bring-up phases.
- **Integrated** WiR wireless stack with Pebble OS application layer, validating wireless data exchange and system stability and reducing bring-up iteration cycles through structured post-silicon test workflows.

Audio Application with WiR Chip Integration Sept 2025 – Jan 2026
Quasistatics Inc.

- **Developed** firmware-level audio application interfacing with the WiR chip, achieving a sidetone latency of 20 ms over WiR wireless communication -meeting real-time audio performance requirements.
- **Configured** and validated end-to-end audio data paths across SPI/I2S interfaces, ensuring stable, low-latency audio streaming and playback on the target hardware platform.

Controlled Bit Error Testing – Baseband Validation Mar 2025 – Jun 2026
Quasistatics Inc.

- **Designed** and implemented a Controlled Bit Error Testing framework targeting the QS127s baseband, validating encoding/decoding integrity and SPI communication under controlled error injection -increasing baseband test coverage by ~40%.
- **Developed** an automated reporting application that surfaced potential IC-level baseband bugs and reduced IC team debug turnaround time, enabling issues previously difficult to reproduce to be isolated and resolved.

System-on-Chip Design - SHA-256 ASIC with Advanced Adder Designs (NYU) Jan 2024 – May 2024
NYU Nano Electronics Lab

- **Contributed** to an open-source ASIC optimized for the SHA-256 hash function (Bitcoin mining), achieving GDS-II tape-out readiness and clearing all DRC/LVS checks by optimizing SDC constraints.
- **Utilized** an advanced adder design that reduced power consumption by 18%, exceeding performance benchmarks from the reference paper.

High Pass Filter Evaluation for Neurotransmitter Drift Mitigation (MS Thesis) Sept 2023 – May 2024
NYU Nano Electronics Lab

- **Designed** a 4-layer PCB for a 256-pin analog IC (dopamine measurement), improving signal integrity by 25% and test efficiency by 80% across 8 independent FSCV channels.
- **Built** firmware and a Python GUI over UART with a custom NIDAQ interface (multithreading/multiprocessing), achieving a 98% success rate in performance validation across all test cycles.

RTL Design - Serial Parallel Multiplier Apr 2024 – May 2024
NYU Nano Electronics Lab

- **Developed** a low-latency, power-efficient Serial Parallel Multiplier in Verilog for SoC integration; executed GDS-II tapeout via OpenLANE, reducing design iterations by 25%.

SRAM BIST Simulation Feb 2023 – May 2023
NYU Nano Electronics Lab

- **Developed** a Verilog RTL design for SRAM with an integrated Built-In Self-Test (BIST) Engine implementing 4 test algorithms; validated using Xilinx Vivado, Synopsys VCS, and Cadence Genus.

SRAM Memory Design and Simulation Nov 2023 – May 2024
NYU Nano Electronics Lab

- **Prototyped** a 1 MB SRAM array using a 7nm PDK in Cadence Virtuoso; synthesized with Cadence Genus to a 50 ns target clock cycle and validated error-detection via Xilinx Vivado, achieving a 98% functional correctness rate.